WE CLAIM:

1. A packaged integrated circuit (IC) device comprising:

a first package part having a top surface and a bottom surface, said top and bottom surfaces having pads for I/O terminals, said first part having connector lines between terminals on said top surface and terminals on said bottom surface;

a cavity in said first package part;

a chip mounted in said cavity, said chip having an active surface including an IC and contact pads;

a second package part having a top surface and a bottom surface, said bottom surface having a first plurality of I/O terminals aligned with said chip contact pads, and a second plurality of I/O terminals aligned with said top surface I/O terminals of said first package part;

said second package part further having connector lines between said first and second plurality of terminals; and

interconnection elements between said chip contact pads and said first plurality of terminals of *said second package part, and between said second* plurality of terminals of said second package part and said top surface terminals of said first package part.

2. The device according to Claim 1 wherein said connector lines in said second package part comprise a signal layer, a power layer, and a ground layer, said layers spaced, respectively, by insulation of a thickness between 10 and 50 μm, and formed into lines having a width less than three times said insulator thickness.

3. The device according to Claim 1 wherein said connector lines in said second package part comprise a signal/power layer and a ground layer, said layers spaced by insulation of a thickness between 10 and 50 μmm, and formed into lines having a width less than three times said insulator thickness.

4. The device according to Claim 1 wherein said chip contact pads are spaced apart by less than 100 μm, center to center.

5. The device according to Claim 1 wherein said interconnection elements between said peripheral chip contact pads and said first plurality of terminals of said second package part are stud bumps.

6. The device according to Claim 5 wherein said stud bumps are selected from a group consisting of gold, copper, copper/nickel/palladium, and alloys thereof.

7. The device according to Claim 1 wherein said interconnection elements between said second plurality of terminals of said second part and said top surface terminals of said first part are reflow interconnections.

8. The device according to Claim 7 wherein said reflow interconnections are made of a material selected from a group consisting of tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, indium, conductive adhesives, and z-axis conductives.

9. The device according to Claim 1 further comprising interconnection elements attached to said bottom surface terminals of said first package part, operable to connect to external parts.

10. The device according to Claim 1 wherein said chip has central contact pads as well as peripheral contact

pads.

11. The device according to Claim 10 wherein said second package part further comprises an opening sized to expose said central chip contact pads, and I/O terminals distributed around said opening, said terminals on said top surface.

12. The device according to Claim 10 wherein said first plurality of bottom I/O terminals of the second package part is aligned with said peripheral chip contact pads.

13. The device according to Claim 10 wherein bonding wires connect said central chip contact pads and said top surface terminals of said second package part.

14. The device according to Claim 10 wherein interconnection elements connect said peripheral chip contact pads and said first plurality of terminals of said second package part, and said second plurality of terminals of said second package part and said top surface terminals of said first package part.

15. The device according to Claim 13 further comprising encapsulation material covering said bonding wires and at least portion of said second package part and of said chip.

16. A packaged integrated circuit (IC) device comprising:

a first package part having a top surface and a bottom surface, said top and bottom surfaces having pads for I/O terminals, said first part having connector lines between terminals on said top surface and terminals on said bottom surface;

a chip mounted on said top surface of said first package part, said chip having an active surface including an IC and contact pads;

a second package part having a top surface and a

bottom surface, said bottom surface having a first plurality of I/O terminals aligned with said chip contact pads, and a second plurality of I/O terminals aligned with said top surface I/O terminals of said first package part;

said second package part further having connector lines between said first and second plurality of terminals; and

interconnection elements between said chip contact pads and said first plurality of terminals of said second package part, and between said second plurality of terminals of said second package part and said top surface terminals of said first package part.

17. The device according to Claim 16 wherein said connector lines in said second package part comprise a signal layer, a power layer, and a ground layer, said layers spaced, respectively, by insulation of a thickness between 10 and 50 μm, and formed into lines having a width less than three times said insulator thickness.

18. The device according to Claim 16 wherein said connector lines in said second package part comprise a signal/power layer and a ground layer, said layers spaced by insulation of a thickness between 10 and 50 μmm, and formed into lines having a width less than three times said insulator thickness.

19. The device according to Claim 16 wherein said chip contact pads are spaced apart by less than 100 μm, center to center.

20. The device according to Claim 16 wherein said interconnection elements between said peripheral chip contact pads and said first plurality of terminals of

said second package part are stud bumps.

21. The device according to Claim 20 wherein said stud bumps are selected from a group consisting of gold, copper, copper/nickel/palladium, and alloys thereof.

22. The device according to Claim 16 wherein said interconnection elements between said second plurality of terminals of said second part and said top surface terminals of said first part are reflow interconnections.

23. The device according to Claim 22 wherein said reflow interconnections are made of a material selected from a group consisting of tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, indium, conductive adhesives, and z-axis conductives.

24. The device according to Claim 16 further comprising interconnection elements attached to said bottom surface terminals of said first package part, operable to connect to external parts.

25. The device according to Claim 16 wherein said chip has central contact pads as well as peripheral contact pads.

26. The device according to Claim 25 wherein said second package part further comprises an opening sized to expose said central chip contact pads, and I/O terminals distributed around said opening, said terminals on said top surface.

27. The device according to Claim 25 wherein said first plurality of bottom I/O terminals of the second package part is aligned with said peripheral chip contact pads.

28. The device according to Claim 25 wherein bonding wires connect said central chip contact pads and said top surface terminals of said second package part.

29. The device according to Claim 25 wherein interconnection elements connect said peripheral chip contact pads and said first plurality of terminals of said second package part, and said second plurality of terminals of said second package part and said top surface terminals of said first package part.

30. The device according to Claim 25 further comprising encapsulation material covering said bonding wires and at least portion of said second package part and of said chip.

31. A method of assembling an IC device, including a chip having an active surface including contact pads, comprising the steps of:

depositing an interconnection element on at least some of said chip contact pads;

providing a first package part having a cavity and I/O terminals on its top surface and its bottom surface;

mounting said chip into said cavity;

providing a second package part having on its bottom surface a first plurality of I/O terminals aligned with said chip contact pads, and a second plurality of I/O terminals aligned with said top surface I/O terminals of said first package part;

connecting said first plurality of I/O terminals of said second package part to said contact pads on said active chip surface; and

connecting said top surface I/O terminals of said first package part with said second plurality of I/O terminal of said second package part.

32. The method according to Claim 31 wherein said step of

depositing an interconnection element comprises plating, electro-plating, sputtering, and evaporating.

33. The method according to Claim 31 further including the step of depositing reflow interconnection material on at least some of said top surface I/O terminals of said first package part.

34. The method according to Claim 33 wherein said step of depositing reflow interconnection material comprises plating, electro-plating, and attaching pre-fabricated units.

35. The method according to Claim 31 wherein said step of connecting said first plurality comprises the method of thermo-compression gang bonding said first plurality I/O terminals of said second package part onto said chip interconnection elements.

36. The method according to Claim 31 further comprising the step of:

underfilling an adhesive non-conductive polymer into any spaces between said chip, said cavity, said second package part, and said interconnection elements, thereby strengthening said assembly.

37. The method according to Claim 31 further comprising the step of:

attaching reflow interconnections to said I/O terminals on said bottom surface of said first package part.

38. The method according to Claim 31 wherein said chip has central contact pads as well as peripheral contact pads.

39. The method according to Claim 38 wherein said second package part comprises an opening sized to expose said central chip contact pads, a top surface and a bottom

surface, said top surface having I/O terminals distributed around said opening, said bottom surface having a first plurality of I/O terminals aligned with said peripheral chip contact pads, and a second plurality of I/O terminals aligned with said top surface I/O terminals of said first package part.

40. The method according to Claim 39 further comprising the step of wire bonding said central chip contact pads to said top surface I/O terminals of said second package part.

41. The method according to Claim 40 further comprising the step of encapsulating, with a polymer compound, said bonding wires and at least portions of said second package part and of said chip.